AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A PLL circuit adapted for reproducing, from an input signal which has been caused to undergo transmission through a desired transmission system, a clock of the input signal, the PLL circuit comprising:

a binarization circuit for bianarizing the input signal to generate a binarized signal;

a signal generating circuit for allowing frequency to be variable by a control signal to output a first oscillating output signal and a second oscillating signal different from the first oscillating output signal by 90 degrees ~~[π/2]~~ (π/2) in phase;

a first phase comparison circuit for performing phase comparison between the first oscillating output signal and the binarized signal to output a first phase comparison result;

a second phase comparison circuit for performing phase comparison between the second oscillating output signal and the binarized signal to output a second phase comparison result;~~,~~

a control direction judgment circuit for judging, on the basis of polarities of the first and second phase comparison results, control direction ~~by~~ of the control signal to output a control direction judgment result;

an integrating circuit for integrating the control direction judgment ~~results~~ result to output an integrated result; and

a correction circuit for discriminating whether or not the integrated result is zero to detect, from ~~the~~ a discrimination result and an output of the first or second phase comparison circuit, that the phase difference is ~~[±π/2]~~ ±π/2 to output a correction-processed control signal in which correction processing has been performed on the basis of ~~the~~ a detection result thus obtained,

whereby to control the operation of the signal generating circuit by the correction-processed control signal to output the clock by the first or second phase comparison result.

2. (Currently Amended) The PLL circuit as set forth in claim 1, wherein the input signal ~~consists of~~ comprises a PSK modulating signal.

3. (Currently Amended) The PLL circuit as set forth in claim 1, wherein the input signal ~~consists of~~ comprises a modulating signal by Manchester code.

4. (Currently Amended) A demodulating circuit adapted for reproducing, from an input signal which has been caused to undergo transmission through a desired transmission system, data sequential caused to undergo transmission through the input signal, the demodulating circuit comprising:

a binarization circuit for binarizing the input signal to generate a binarized signal;

a signal generating circuit for allowing frequency to be variable by a control signal to output a first oscillating output signal and a second oscillating output signal different from the first oscillating output signal by 90 degrees ~~[π/2]~~ (π/2) in phase;

a first phase comparison circuit for performing phase comparison between the first oscillating output signal and the binarized signal to output a first phase comparison result;

a second phase comparison circuit for performing phase comparison between the second oscillating signal and the binarized signal to output a second phase comparison result;

a control direction judgment circuit for judging control direction ~~by~~ of the control signal on the basis of polarities of the first and second phase comparison results to output control direction judgment result;

an integrating circuit for integrating the control direction judgment results by one period of the input signal to output an integrated result; and

a correction circuit for discriminating whether or not the integrated result is zero to detect, from ~~the~~ a discrimination result and an output of the first or second phase comparison circuit, that the phase difference is ~~[±π/2]~~ ±π/2 to output a correction-processed control signal in which correction processing has been performed on the basis of ~~the~~ a detection result thus obtained,

whereby to control the operation of the signal generating circuit by the correction-processed control signal to output the data sequential by the first or second phase comparison result.

5. (Currently Amended) The demodulating circuit as set forth in claim 4, wherein the input signal ~~consists of~~ comprises a PSK modulating signal.

6. (Currently Amended) The demodulating circuit as set forth in claim ~~5~~ 4, wherein the input signal ~~consists of~~ comprises a modulating signal by Manchester code.

7. (Currently Amended) An IC card adapted for demodulating data sequential, by a demodulating circuit, from a transmit signal which has been received through an antenna to process the demodulated data sequential thus obtained, the demodulating circuit comprising:

a binarization circuit for binarizing the transmit signal to generate a binarized signal;

a signal generating circuit for allowing frequency to be variable by a control signal to output a first oscillating output signal and a second oscillating output signal different from the first oscillating output signal by 90 degrees ~~[π/2]~~ (π/2) in phase;

a first phase comparison circuit for performing phase comparison between the first oscillating output signal and the binarized signal to output a first phase comparison result;

a second phase comparison circuit for performing phase comparison between the second oscillating output signal and the binarized signal to output a second phase comparison result;

a control direction judgment circuit for judging control direction ~~by~~ of the control signal on the basis of polarities of the first and second phase comparison results to output control direction judgment result;

an integrating circuit for integrating the control direction judgment ~~results~~ result by one period of the ~~input~~ transmit signal to output an integrated result; and

a correction circuit for discriminating whether or not the integrated result is zero to detect, from ~~the~~ a discrimination result and an output of the first or second phase comparison circuit that the phase difference is ~~[±π/2]~~ ±π/2 to output a correction-processed control signal in which correction processing has been performed on the basis of ~~the~~ a detection result thus obtained,

whereby to control the operation of the signal generating circuit by the correction-processed control signal to output the data sequential by the first or second phase comparison result.

8. (Currently Amended) The IC card as set forth in claim 7, wherein the transmit signal ~~consists of~~ comprises a PSK modulating signal.

9. (Currently Amended) The IC card as set forth in claim 7, wherein the transmit signal ~~consists of~~ comprises a modulating signal by Manchester code.

10. (Currently Amended) An IC card processing apparatus adapted for demodulating, from a response signal which has been received through an antenna, data sequential which has been sent out from an IC card by using a demodulating circuit to process the data sequential thus demodulated, the demodulating circuit comprising:

a binarization circuit for binarizing the response signal to generate a binarized signal;

a signal generating circuit for allowing frequency to be variable by a control signal to output a first oscillating output signal and a second oscillating output signal different from the first first output signal by 90 degrees ~~[π/2]~~ (π/2) in phase;

a first phase comparison circuit for performing phase comparison between the first oscillating output signal and the binarized signal to output a first phase comparison result;

a second phase comparison circuit for performing phase comparison between the second oscillating output signal and the binarized signal to output a second phase comparison result; a control direction judgment circuit for judging control direction ~~by~~ of the control signal on the basis of polarities of the first and second phase comparison results to output control direction judgment result;

an integrating circuit for integrating the control direction judgment ~~results~~ result by one period of the ~~input~~ response signal to output an integrated result; and

a correction circuit for discriminating whether or not the integrated result is zero to detect, from ~~the~~ a discrimination result and an output of the first or second phase comparison circuit, that the phase difference is ~~[±π/2]~~ ±π/2 to output a correction-processed control signal in which correction processing has been performed on the basis of ~~the~~ a detection result thus obtained,

whereby to control the operation of the signal generating circuit by the correction-processed control signal to output the data sequential by the first or second phase comparison result.

11. (Currently Amended) The IC card processing apparatus as set forth in claim 10, wherein the response signal ~~consists of~~ comprises a PSK modulating signal.

12. (Currently Amended) The IC card processing apparatus as set forth in claim 10, wherein the response signal ~~consists of~~ comprises a modulating signal by Manchester code.